IN THE CLAIMS:

Please amend claims 12 and 14 as follows:

1. – 4. (Canceled)

5. (Previously amended) A high-voltage MOS transistor wherein a dopant concentration of a source offset region is set lower than a dopant concentration of a drain offset region and thereby a resistance value of the source region is set independently of a resistance value of the drain region in such a manner as to maintain a high sustaining breakdown voltage of the high-voltage MOS transistor, which is based on a voltage of the source offset region and a voltage of a substrate region directly under a gate insulating film during operation of the high-voltage MOS transistor.

C2 fig. 4

6. – 7. (Canceled)

8. (Withdrawn) A method for fabricating a high-voltage MOS transistor, comprising the steps of:

defining a resist pattern that makes a size of a source offset region greater than a size of a drain offset region; and

forming the source and drain offset regions using the resist pattern to increase a sustaining breakdown voltage of the transistor.

9. (Withdrawn) A method for fabricating a high-voltage MOS transistor, comprising the steps of:

forming a drain offset region; and

forming a source offset region by implanting dopant ions at such a level as setting a dopant concentration of the source offset region independently of a dopant

concentration of the drain offset region to increase a sustaining breakdown voltage of the transistor.

10. (Withdrawn) The method of Claim 9, wherein the dopant concentration of the source offset region is set lower than that of the drain offset region.

12. (Currently amended) A high-voltage MOS transistor wherein a dopant concentration of a source offset region is set lower that a dopant concentration of a drain offset region such that the following inequality is not ~~easily~~ satisfied during operation of the high-voltage MOS transistor:

C2 Cont.

VW – (a forward biased breakdown voltage of silicon) > VS

fig. 4, 10(a) p. 32-33

where, VW is a substrate voltage of a substrate region directly under a gate insulating film, and VS is a source voltage of the source offset region, and thereby a resistance value of the source offset region is set independently of a resistance value of the drain offset region in such a manner as to maintain a high sustaining breakdown voltage of the high-voltage MOS transistor, which is based on a voltage of the source offset region and a voltage of the substrate region directly under a gate insulating film during operation of the high-voltage MOS transistor.

13. (Original) A high-voltage MOS transistor wherein a length of a region overlapping between a source offset region and a source well offset region is set smaller than a length of a region overlapping between a drain offset region and a drain well offset region and thereby a resistance value of source offset region is set independently of a resistance value of the drain offset region in such a manner as to maintain a high-sustaining breakdown voltage of the high-voltage MOS transistor, which is based on a voltage of the source offset region and a voltage of a substrate region directly under a gate insulating film during operation of the high-voltage MOS transistor.

fig. 1, 7

14. (Currently amended) A high-voltage MOS transistor wherein a length of a region overlapping between a source offset region and a source well offset region is set smaller than a length of a region overlapping between a drain offset region and a drain well offset region such that the following inequality is not ~~easily~~ satisfied during operation of the high-voltage MOS transistor:

C2
fig. 1, 7, 10(a),
P, 24, 25
42

VW – (a forward biased breakdown voltage of silicon) > VS

where VW is a substrate voltage of a substrate region directly under a gate insulating film and VS is a source voltage of the source offset region, and thereby a resistance value of the source offset region is set independently of a resistance value of the drain offset region in such a manner as to maintain a high sustaining breakdown voltage of the high-voltage MOS transistor, which is based on a voltage of the source offset region and a voltage of the substrate region directly under a gate insulating film during operation of the high-voltage MOS transistor.